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DATE MAILED: 12/13/95

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☑ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☑ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☑ Claims 1-25 are pending in the application.

   Of the above, claims _____ are withdrawn from consideration.

2. ☐ Claims _____ have been cancelled.

3. ☐ Claims _____ are allowed.

4. ☑ Claims 1-25 are rejected.

5. ☐ Claims _____ are objected to.

6. ☐ Claims _____ are subject to restriction or election requirement.

7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.

8. ☐ Formal drawings are required in response to this Office action.

9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).

10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).

11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).

12. ☑ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☑ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____.

13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14. ☐ Other

EXAMINER'S ACTION

Part III DETAILED ACTION

European Search Report on PTO-1449 has not been considered because it is not a published document.

Drawings

1. The drawings are objected to because Figures 1-2 are not designated by a legend such as "Prior Art". The legend is necessary in order to clarify what applicant's invention is. MPEP § 608.02(g). Correction is required.

2. The drawings are objected to because of the following informalities: the P channel transistors M1 and M3 on Figs. 2-3 and 5 are not properly drawn as to distinguish them from N channel transistors - it is suggested that empty dots be drawn at the gates of the PFETs; and the polarities of bulk diodes D1-D4 as shown on Figs. 3 and 5 are incorrect. Correction is required.

3. The drawings are objected to under 37 C.F.R. § 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "inverting buffer" and "non-inverting buffer" in claim 12 must be shown or the feature cancelled from the claim. No new matter should be entered.

Specification

4. The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The specification is objected to under 35 U.S.C. § 112, first paragraph, as failing to provide an enabling disclosure. It's not clear how the output OUT on Fig. 3 would rise to "2*VS-S*VD-2*RD*IL-IL*T/C" with only a bridge of the diodes D1-D4 in the absence of the MOS transistors as described on page 4; since the polarities of diodes as shown on Figs. 3 and 5 are drawn opposite to what they really are, it is not clear how charge can be transferred to the capacitor SC from nodes NA and NB via diodes D1 and D3. For example, a PFET has its bulk diodes' cathode connected to source/drain terminals.

Claim Rejections - 35 USC § 112

5. Claims 1-25 are rejected under 35 U.S.C. § 112, first paragraph, for the reasons set forth in the objection to the specification.

6. Claims 1-25 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Numerous problems, too many to mention individually, are present in the claims. Examples of such

deficiencies are described hereinafter. In claims 1-3,7 and 9, the phrase "as to..." does not positively recite a circuit function. In claims 2 and 9, the transistors M1-M4 on Fig. 3 creating "a one-way conduction path between said negative terminals and said positive terminals of said inverters" are indefinite because, when the parasitic diodes of the transistors are conducting, the corresponding transistors are conducting also so that two way conduction path is established between the drain and source of respective transistors. Furthermore, there is no "conduction path" between the positive terminal connected to SC on Fig. 3 and the negative terminal connected to VS because transistors M3 and M1 are turned on and off alternatingly with transistors M2 and M4. In claims 3,5,21-22, the voltage doubler having separate "four diodes" and separate "four transistors" is indefinite because the "bulk diodes" are a part of the four transistors and they are known to be parasitic so that claiming them as if they are discrete elements is incorrect. In claim 3, the terms "the voltage drop" and "the bridge branches" lack antecedent basis. In claims 6 and 13-14, the second occurrence of the term "a continuous power voltage" is indefinite about whether it is referring to the same voltage mentioned before or another voltage. The term "indifferent terminals" is vague as to what it means and lacks an antecedent basis from the specification; it's not clear why the terminals NB and NA on Fig. 3 are indifferent from each other. The terms "the value" and

"said second potential" lack antecedent basis. The term "number of the at least one charging section" is indefinite because a section does not have a number. The output corresponding to "...potential less the value... plus the product of... voltage" is indefinite because the potential, value and voltage are not same physical quantities that can be added to and subtracted from each other and validity of the addition and subtraction to obtain the output is questioned because the term "said second potential" lacks an antecedent basis. In claim 11, the term "said first input terminal" lacks an antecedent basis. In claim 12, it is suggested that the phrase "and from a non-inverting buffer" be changed to " and a single output from a non-inverting buffer" for clarity. In claim 13, the programmable non-volatile memory device is indefinite because the circuits on Figs. 3-6 are not "programmable... non-volatile memory devices". It is suggested that the term "powerable" be changed to a more positive word such as "powered". The term "delectable" is not a word. In claims 13-14, the terms "the type", "said continuous power voltage", "the output of the booster" lack antecedent basis. In claim 14, it is not understood what's meant by the phrase "hold... with changes". The term "the operating conditions" lacks an antecedent basis. In claim 18, the term "the constant voltage" is indefinite about which one of the two constant voltages that the term is referring to. In claim 20, it is suggested that the terms "one output" and "another output" be changed to "said one

output" and "said another output" to indicate that they have antecedent basis. In claims 21-22, it is suggested that the phrase "terminal is the..." be changed to "terminal is connected to the..." for clarity. The terms "the output" and "the input" are indefinite about which elements that the input and output are terminals of. The "two indifferent terminals" are indefinite for the reason discussed above. In claim 23, it is suggested that the "lower... voltage" be changed to "low... voltage" for clarity. In claim 24, the second occurrent of the term "an output voltage" of the charge transfers capacitors fails to show that it has an antecedent basis. The phrase "providing said output voltage at" is indefinite about which element the output voltage is a voltage of. In claim 25, it is suggested that the terms "a first" and "a last" be changed to "a first bridge circuit" and "a last bridge circuit" for clarity. The phrase "as the output voltage" is indefinite about which element the output voltage is a voltage of.

7. Claim 11 is rejected under 35 U.S.C. § 112, fourth paragraph, as being of improper dependent form for failing to further limit the subject matter of a previous claim.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section

> 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

9. Claims 1-25 are rejected under 35 U.S.C. § 103 as being unpatentable over Matsumura, as far as understood from the languages of the claims. With respect to claim 1-2,23-24, Matsumura discloses on Fig. 4 a circuit comprising:

oscillator 44 on Fig. 3 having first and second outputs at nodes R1,S1 on Fig. 4;

first charge transfer capacitor 11 on Fig. 4; and

second charge transfer capacitor 12. The inherent capacitance of the substrate would have worked as a charge accumulation capacitor. Matsumura fails to disclose two inverters. However, it is notoriously well known in the art that the diodes in a charge pump can be replaced with switching transistors in order to reduce voltage loss across the diodes. In Matsumura's circuit, since the transistor 13 is supposed to conduct current at times out of phase with 15 by 180 degrees and it had to be connected to a clock signal other than the one at P1 so that 13 would not form a diode, connecting the gate of the

transistor 13 in common with the gate of 15 and changing the transistor 13 to a opposite type from 15 would have been an obvious design implementation in changing the diode 13 to a switching transistor, wherein two groups of transistors, (13,15) and (14,16), would have formed two inverters connected to the charge transfer capacitors.

Therefore, it would have been obvious to a person of ordinary skills in the art at the time of invention to change the diodes 13,14 of Matsumura to switching transistors to thereby form parts of two inverters in order to reduce voltage loss across the diodes, as called for in claims 1-2,23-24.

With respect to claims 3-11,13-14, the transistors 13-16 have parasitic bulk diodes. For claim 12, the oscillator provides outputs from a non-inverting buffer 17-20 and an inverting buffer 21-22.

With respect to claims 15,17-19,21, it is notoriously well known in the art that a charge pump used to generate a substrate bias voltage which is a negative voltage can be used with little modifications to generate a positive voltage which is a multiple of the supply voltage provided to the charge pump. For example, Okada discloses on lines 48-56 of column 6 that such modifications can be made to produce a positive voltage "above the power source potential". Therefore, it would have been obvious to a person of ordinary skills in the art at the time of invention to use the charge pump of Matsumura to produce a

positive voltage which is a multiple of the provided supply voltage by making little modifications to the circuit in order to provide a high voltage used in memory devices, as called for in claims 15,17-19,21.

With respect to claim 16, it would have been obvious to use a capacitor at the output of the charge pump to stabilize the output. With respect to claim 20,22, it is notoriously well known in the art that a multiple stages of charge pumps can be used in series. Therefore, it would have been obvious to a person of ordinary skills in the art at the time of invention to use a multiple stages of charge pump of Matsumura to produce a high voltage for use in a memory device, as called for in claims 20,22,25.

10. Claims 1-25 are rejected under 35 U.S.C. § 103 as being unpatentable over Okada, as far as understood from the languages of the claims. With respect to claim 1-2,23-24, Okada discloses on Fig. 2A a circuit comprising:

oscillator 1,2 on Fig. 2A;

first charge transfer capacitor C1; and

second charge transfer capacitor C2. The inherent capacitance of the substrate would have worked as a charge accumulation capacitor. Okada fails to disclose two inverters. However, it is notoriously well known in the art that the diodes in a charge pump can be replaced with switching transistors in order to reduce voltage loss across the diodes. In Okada's

circuit, since the transistor TD1 is supposed to conduct current at times that are out of phase with T1 by 180 degrees and it had to be connected to a clock signal other than the one at P1 so that TD1 would not form a diode, connecting the gate of the transistor TD1 in common with the gate of T1 and changing the transistor TD1 to a opposite type from T1 would have been an obvious design implementation in changing the diode TD1 to a switching transistor, wherein two groups of transistors, (T1,TD1) and (T2,TD2), would have formed two inverters connected to the charge transfer capacitors.

Therefore, it would have been obvious to a person of ordinary skills in the art at the time of invention to change the diodes TD1-TD2 of Okada to switching transistors to thereby form parts of two inverters in order to reduce voltage loss across the diodes, as called for in claims 1-2,23-24.

With respect to claims 3-11,13-14, the transistors T1,T2,TD1,TD2 have parasitic bulk diodes. For claim 12, the oscillator provides outputs from a non-inverting buffer 1 and an inverting buffer 2.

With respect to claims 15,17-19,21, Okada discloses on lines 48-56 of column 6 that such modifications can be made to produce a positive voltage "above the power source potential". Okada's circuit could have produced a positive voltage which is a multiple of the provided supply voltage by making little modifications, as called for in claims 15,17-19,21.

With respect to claim 16, it would have been obvious to use a capacitor at the output of the charge pump to stabilize the output. With respect to claim 20,22, it is notoriously well known in the art that a multiple stages of charge pumps can be used in series. Therefore, it would have been obvious to a person of ordinary skills in the art at the time of invention to use a multiple stages of charge pump of Matsumura to produce a high voltage for use in a memory device, as called for in claims 20,22,25.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Jung Kim whose telephone number is (703) 305-7242. The Art Unit 2504's FAX number is (703)308-7722.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956.

JK
December 7, 1995

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SUPERVISORY PATENT EXAMINER
GROUP 2500